

A “Snapshot” of AlGaIn/GaN HEMT State-of-the-Technology

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Abstract

The Defense Advanced Research Projects Agency (DARPA) is currently sponsoring a Wide Band Gap Semiconductor Technology Initiative (WBGSTI). The objective of this program, managed by Edgar Martinez and Mark Rosker, is four-fold: (1) to scale (up to 4”) high quality SiC substrates, (2) to develop alternative substrates, (3) to develop uniform AlGaIn/GaN High Electron Mobility Transistor (HEMT) epitaxial growth, and (4) to examine materials/device correlations. This paper will present measured AlGaIn/GaN HEMT device results that provide a snapshot of the State-of-the-Technology with respect to this DARPA program.

INTRODUCTION

As part of this program, the Air Force Research Laboratory (AFRL), Army Research Laboratory (ARL), and Naval Research Laboratory (NRL) have joined to form a Tri-Service Support Team. The Tri-Service Team, led by Tom Jenkins of AFRL, is composed of a Materials Panel and a Device Panel (Figure 1). Briefly, the Materials Panel is responsible for analyzing substrates and epitaxy with respect to program goals through electrical, structural and optical characterization. The Device Panel examines processed deliverables, wafers with fabricated devices. Extensive electrical characterization including full wafer DC and small-signal RF screening, as well as, power and noise sampling of transistors and test structures is performed. This presentation will focus on testing, characterization and observations from the device panel.

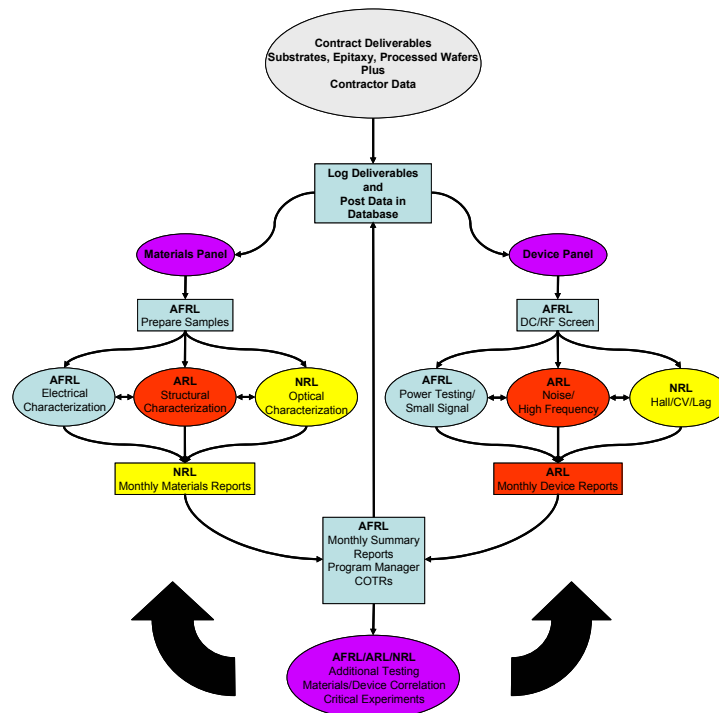


Figure 1 Tri-Service Support Team Activities

TESTING

A DoD test reticle (Figure 2) including both process control monitor structures (TLM, VDP, CV, etc) and small active devices (0.3 mm, FATFET) is included on processed deliverables. Standard test procedures are applied to obtain material characteristics, DC parameters, and RF performance. DC and small-signal RF screening is performed on all wafers via automated test routines at the wafer scale (up to 500 sites or more per wafer). Materials characterization, large-signal analysis and noise measurements are performed on a limited number of sites per wafer on a subset of all the processed deliverables. For example, mobility, sheet charge and AlGaN thickness values are obtained from on-wafer Hall and CV measurements.

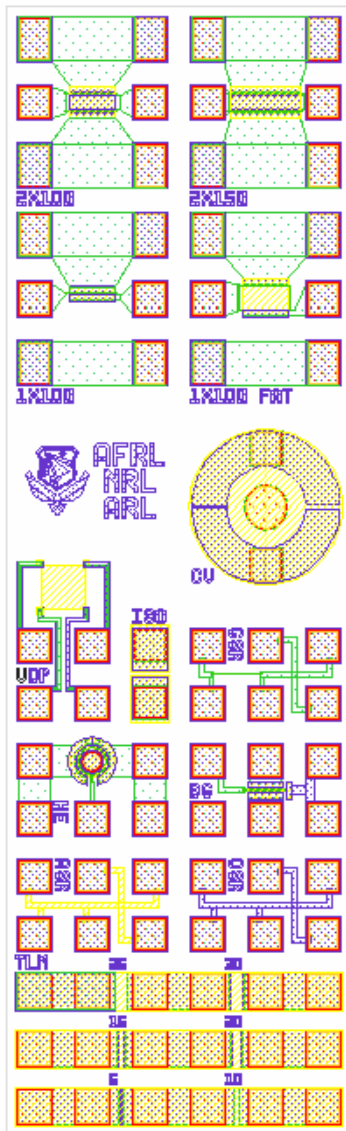


Figure 2 DoD Test Reticle

Over 100 wafers (combination of 2” and 3” SiC substrates) from six different epi sources, both MBE and MOCVD, which were processed at several different foundries, have been characterized to date. Test conditions for select parameters being measured by the Tri-Service team are shown in Table 1. For parameters measured via the automated test routines, wafermaps (Figure 3) are generated from the raw data to obtain statistics (average and standard deviation) as well as gauge the yield and “goodness” of the data. For other parameters (material characteristics and power) simple spreadsheet routines are used to obtain statistics.

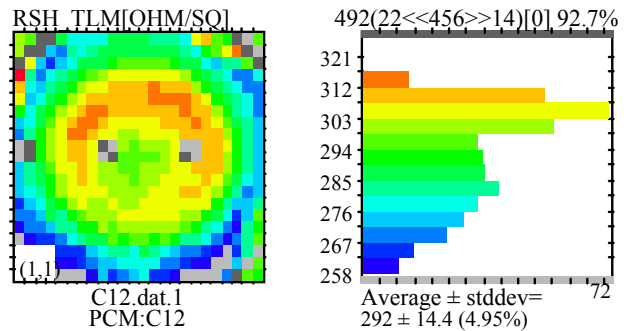


Figure 3 Sample Wafermap with Statistics

The range (minimum and maximum values) in observed data as well as the median and average values for select parameters can be seen in Table 2. Summary charts showing wafer averages and standard deviations for all wafers tested will be presented. An example is seen in Figure 4. These are not trend charts as material structures and device fabrication processes are continuing to undergo optimization. Nor are they intended as direct comparison charts as a standard epi-structure and/or process is not being applied. What can be gleaned from these charts is an assessment of the state-of-the-technology. What are global vs. local issues? Is there a difference between growth techniques (MBE vs. MOCVD)? What is the range of values for a given material or device parameter? Does it vary across wafer lots? Is device parameter uniformity (standard deviation) improving with respect to material and process optimization efforts?

Table 1 Test Conditions

Parameter	Descriptor	Structure	Conditions
μ	Mobility	Van Der Pauw	On wafer Hall measurement. Magnetic field = 2000 Gauss, test current typically 100 μ A
Nsh	Sheet Charge	Van Der Pauw	On wafer Hall measurement. Magnetic field = 2000 Gauss, test current typically 100 μ A
AlGaIn d	AlGaIn Thickness	CV	Zero bias capacitance measurement. (1 MHz)
RSH_TLM	Sheet Resistance (Active Layer)	TLM	Force 1 mA each gap, measure voltage using Kelvin technique. Calculate from curve fit to data.
IISO_50V	Buffer Isolation Current	Isolation	Force 50 V, measure current between 5 μ m gap.
VISO_100nA	Isolation Voltage @ 100 nA	Isolation	Force 100 nA, measure voltage between 5 μ m gap.
VISO_10 μ A	Isolation Voltage @ 10 μ A	Isolation	Force 10 μ A, measure voltage between 5 μ m gap.
Idss	Ids for Vgs = 0V at Vds = 10V	2x150 Transistor	Measured from Gm, Id vs. Vgs curve.
Imax	Ids for Vgs = 1V at Vds = 10V	2x150 Transistor	Measured from Gm, Id vs. Vgs curve.
Vth	Threshold Voltage	2x150 Transistor	Measured from IV curve.
Igl	Gate Leakage	2x150 Transistor	Ig where Vds = 10 V, Vgs = Vth - 2 V.
Rc	Ohmic Contact Resistance	TLM	Force 1 mA each gap, measure voltage using Kelvin technique. Calculate from curve fit to data.
GmP	Peak Transconductance	2x150 Transistor	Measured from Gm, Id vs. Vgs curve.
Ft	Cutoff Frequency @ GmP	2x150 Transistor	s-parameters
Glag	Gate Lag	2x150 Transistor	Vds = 1 V, Vgs swept from Vth - 2 V to 0 V. Ratio of pulsed/dc current.
Dlag	Drain Lag	2x150 Transistor	Vds = 0.1 V, 20 V, 0.1 V with Vgs = 0 V. Ratio of ending/starting drain current.
P1dB	Output Power @ 1 dB Compression	2x150 Transistor	Optimized for power where Vds = 15 V, Vgs = 30% Idss.
Gp	Gain @ 1 dB Compression	2x150 Transistor	Optimized for power where Vds = 15 V, Vgs = 30% Idss.
PAE	Peak Power Added Efficiency	2x150 Transistor	Optimized for power where Vds = 15 V, Vgs = 30% Idss.

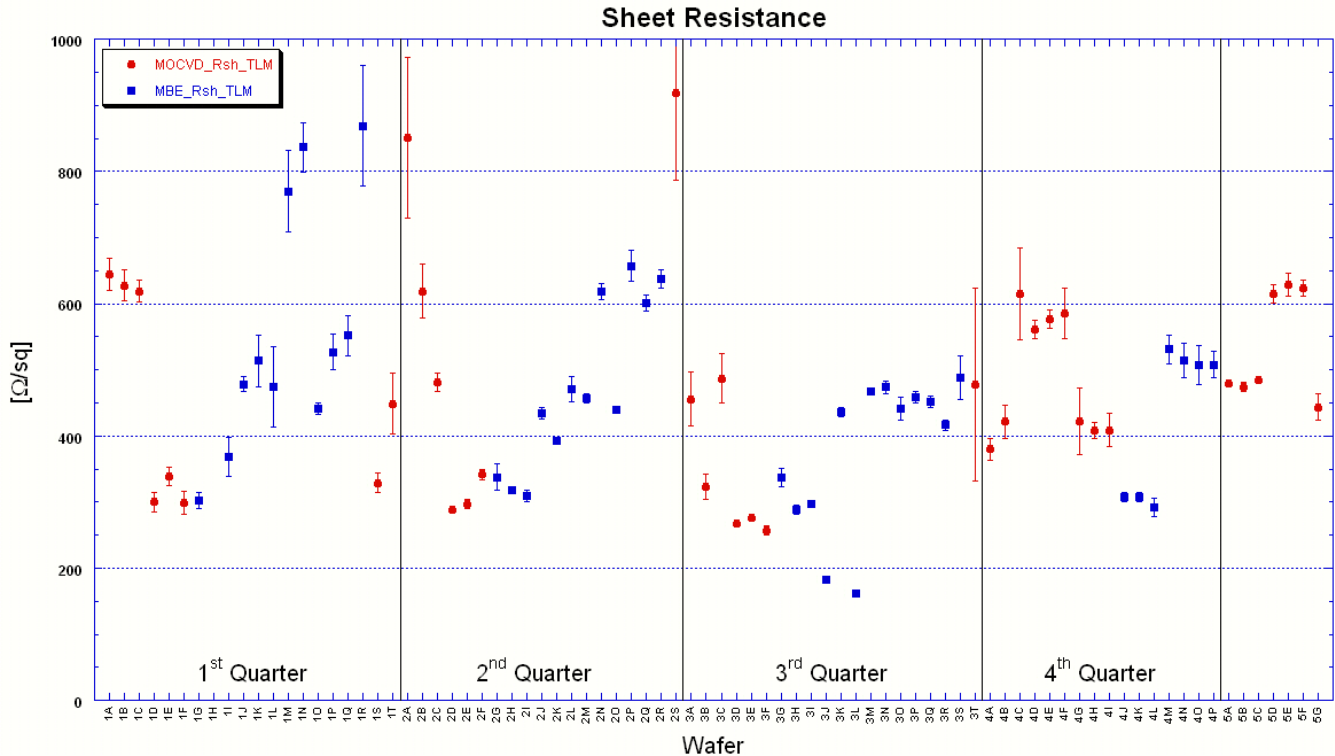


Figure 4 Sample Summary Chart

Table 2 Summary Data

Parameter	Minimum	Maximum	Median	Average
μ [cm ² /V*s]	632	2027	1351	1317.73
Nsh (e13) [cm-2]	0.41	6	1.15	1.25
AlGaN Thick [Å]	127	333	235	236.43
Rsh_TLM [Ω/sq]	162	918	457	466.20
IISO @ 50V [A]	1.02E-09	9.25E+01	3.35E-06	1.14E+00
VISO @ 100nA [V]	0.00065	60	9.87	24.43
VISO @ 10uA [V]	0.0857	60	59.5	40.05
Idss [mA/mm]	254	1330	793	838.69
Imax [mA/mm]	396	1420	968	986.98
Vth [V]	-6.82	-0.783	-3.725	-4.00
AB_igl [mA/mm]	2.34E-05	50.5	0.2575	3.17
Rc [Ω-mm]	0.0976	3.14	0.516	0.68
GMP [mS/mm]	118	407	235	246.48
Fmax/Ft	0.73	3.15	1.72	1.77
Glag	0.7	1.07	0.92	0.92
Dlag	0.56	1.04	0.91	0.88
P1dB [dBm]	19.86	27.59	25.30	24.81
Gp @ 1dB [dB]	7.90	16.16	12.92	12.86
PAE [%]	25.68	46.36	36.20	36.28

CONCLUSIONS

Significant progress has been made during Phase I of the WBGSTI program. Sheet resistance uniformity and mobility goals have been met on 3" wafers. While there are no specific device performance goals associated with the program, improvements with respect to uniformity (standard deviation) and repeatability (wafer-to-wafer averages) have been observed. Poor buffer isolation characteristics seen early in the program have for the most part been solved. Likewise, gate leakage present in the early deliverables has been reduced. High frequency response has been demonstrated and good power performance observed.

As will be evidenced by the State-of-the-Technology "snapshot" to be presented, the WBGSTI program has successfully established a 3" SiC substrate, AlGaIn/GaN HEMT epitaxy and process capability.

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ACRONYMS

DARPA – Defence Advanced Research Projects Agency
 WBGSTI – Wide Bandgap Semiconductor Technology Initiative
 HEMT – High Electron Mobility Transistor
 AFRL – Air Force Research Laboratory
 NRL – Naval Research Laboratory
 ARL – Army Research Laboratory
 TLM – Transfer Length Method
 VDP – Van Der Pauw
 CV – Capacitance Voltage
 MBE – Molecular Beam Epitaxy
 MOCVD – Metal Organic Chemical Vapor Deposition