# Stepper-based integrated process on wafer pieces.

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## ABSTRACT

**High-cost compound semiconductors involve complicated technological development. Using pieces of a whole wafer allows performing the R&D process in a cost-effective way. We developed a method for the processing a piece of wafer using standard manufacturing equipment. This method provides the benefits of high-resolution and superior alignment capability of a stepper with the low-cost advantages of working with wafer pieces that normally cannot be exposed in a stepper. This article describes what we do in order to allow processing of mounted InP piece in regular FAB equipment.**

## INTRODUCTION

The use of pieces of wafer, or small-size wafer, when developing a process is sometimes a necessity. It is especially common during the R&D phase because it is a cost-effective way, when high-cost materials are in use and many methods of processing are being be tried out. It is also typically the situation when new materials are introduced and wafer size is relatively smaller than those used in the compound semiconductor industry. There are two approaches to perform the full range of microelectronic processes on a piece: use special equipment that can handle pieces, or fit a piece to work with existing tools. One of the most complicated processes is processing lithography on pieces. In most cases, lithography on a piece is limited to mask aligner only, but this tool has its known limitations in resolution, alignment ability, and contact inherent problems [1,2]. Although there are few steppers types which can perform lithography on a piece if it is mounted on a special carrier tool, this solution requires purchasing a separate stepper and is therefore impractical. In this article, we offer a method of using a standard inline stepper to expose pieces as part of an integrated multi-layer process.

We glue a piece of InP wafer to a carrier wafer that was prepared with global and local alignment marks. This approach enables us to use the Nikon stepper in standard operational mode.

## METHOD OVERVIEW

Our goal is to develop a way to perform a multi-layer stepper based process on a piece of epitaxial wafer (InP) glued on a carrier wafer.

The method is based on the idea that the piece is glued permanently to the carrier wafer and the alignment is done intentionally to the carrier only. During the alignment sequence, the stepper is not 'aware' to the presence of the piece and performs its normal operational sequences. Only during the exposure sequence the stepper is focusing locally, prior to each field exposure, thus focusing specifically on the plane of the piece.

Following lithographic steps in the integrated process align to the carrier wafer and expose same locations on the piece, within normal stepper alignment specifications.

This method generates new technological challenges, which we explain below.

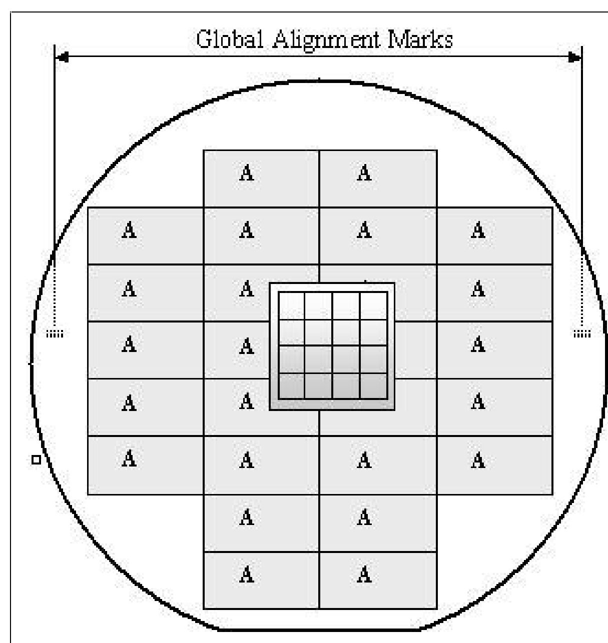



FIGURE 1. Exposure fields on the carrier wafer and the piece.

## METHOD DETAILS

### *PIECES MOUNTING ON CARRIER WAFER*

Choosing the right glue materials is crucial for the success of the process. The glue material must survive thermal budget of 250$^{o}$C and be stable in acids, solvents, and

plasma processes. Only few epoxy-based types of glue are suitable for this application [3].

We select the carrier wafer material according to the mechanical and thermal properties. The preferred material is the one that is less fragile. The difference in wafer and piece thermal expansion coefficients (Table 1) should be as small as possible to prevent the creation of thermally induced stresses. The shape of carrier wafer backside indicates the rate of thermal stress. Only using of GaAs as carrier wafer is adequate for the process (figure 2).

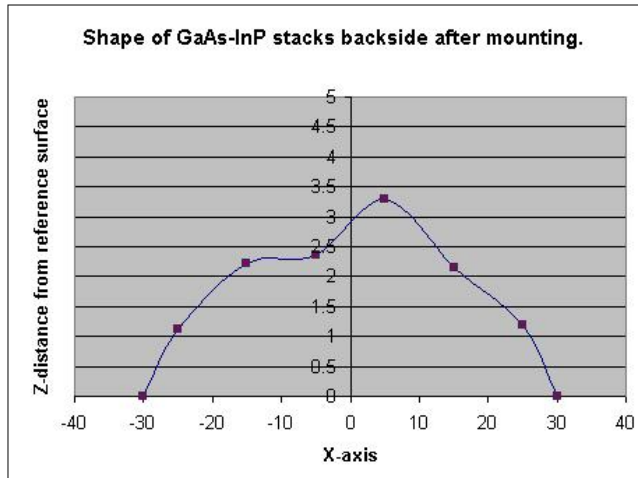



FIGURE 2. Calculated distance from GaAs-InP stack backside along diameter line (bow) to wafer stage (zero height)

3" GaAs Carrier wafer with metalized alignment marks was prepared. Epitaxial InP piece, size 18x18mm, is then glued to the carrier wafer. The precise location of glued piece is not critical, but alignment between the piece and the carrier wafer crystallographic directions is necessary, due to anisotropic nature of InP wet etch. We use metal patterns on the carrier wafers as reference mark for piece alignment. We make location and angular corrections under the microscope of Micrometric measurement tool, keeping angle error lower than $0.06^{o}$. After alignment, curing of epoxy is done under increased temperature and pressure conditions. Stack parallelism measurements done on 30 wafers are presented in figure 3.

TABLE 1
DIFFERENT MATERIALS THERMAL EXPANTION COEFFICIENTS.

| Material | Thermal expansion, linear (°C $^{-1}$) |
|---|---|
| InP | 4.60·10-6 |
| GaAs | 5.73·10-6 |
| Si | 2.6·10-6 |
| Al2O3 (sapphire) | 5.60·10-6 |
| 3C-SiC | 2.77 (42)·10-6 |
| Epoxy glue | ≈2x10-6 |

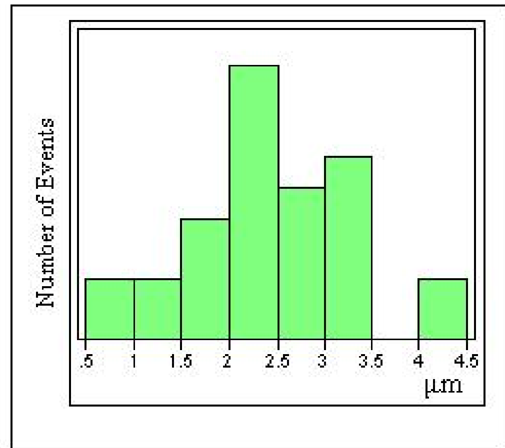



FIGURE 3. Distributions of range of carrier + piece thickness. Mean range (uniformity of mounting) is 2.43, Sigma 0.88.

### *ALIGNMENT*

After gluing, carrier wafer and piece are treated as standard wafer in process. For coating and developing we use Karl Suss ACS-200 cluster tool, for exposure, Nikon body 7 I line stepper. To perform alignment on standard wafer, the stepper needs a couple of global alignment marks and several within-field-alignment-marks [4-6]. We do the same for the carrier wafer, except that the fields we use for alignment surrounds the location of the glued piece, keeping a safe distance from it, to prevent from glue and other obstacles to harm the delicate alignment marks. Alignment results are well within specs of stepper (0.13µm, 3σ).

### *EXPOSURE FIELD SIZE*

Use of GaAs as a carrier wafer gives good results, as explained in previous paragraphs, but still causes some surface deformations of the piece after thermal steps. These deformations are critical when the stepper is involved in exposure due to its shallow depth of focus. In our stepper DOF is +/- 0.9um while measured topographic deformation was up to 4um (figure 3). When the field is exposed, the stepper performs its focus sequence to the center of the field. For large fields exposed on deformed surfaces, topographic variation is detrimental to the lithography resolution and CD within exposure field. Our solution is to design small exposure fields (4x4mm) located only at the center of the reticle, where the machine performs its focus. In this way we obtain a local focus on InP surface for each exposure field, within the DOF of the stepper, receiving the standard deviation of 0.04 for 0.8um CD lines. Figure 4 shows the situation before and after this solution.

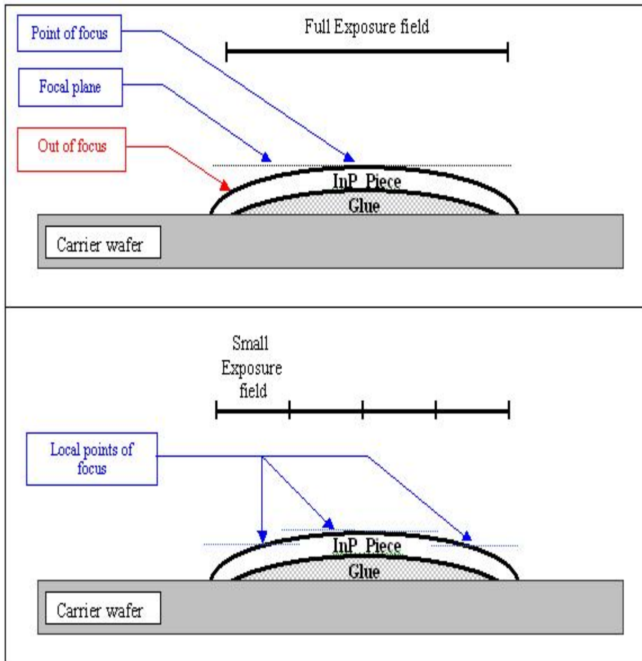



FIGURE 4. Focus and out of focus planes in full field exposure (top) and Local focus planes for small exposure field (bottom).

### *TOTAL THICKNESS*

While exposing the piece and the carrier wafer stack we came across another limitation of the Nikon Stepper; the total thickness of the stack cannot exceed 1200um, or else the total focus travel of the stage prevents the tool from arriving at focus conditions and the stepper aborts the job, resulting in an error. The solution is, if possible, to order an epitaxial InP wafer which is thinner than 450um. Another possibility that we tested successfully is to grind the epitaxial wafer's backside until we reach the desired overall thickness prior to InP wafer dicing. Reducing carrier wafers thickness instead is not recommended, since it may harm the flatness uniformity, resulting in reduced stepper performance. Thinner carrier wafers are more likely to deform during gluing, and break throughout the process.

### *LIFT OFF LITHOGRAPHY*

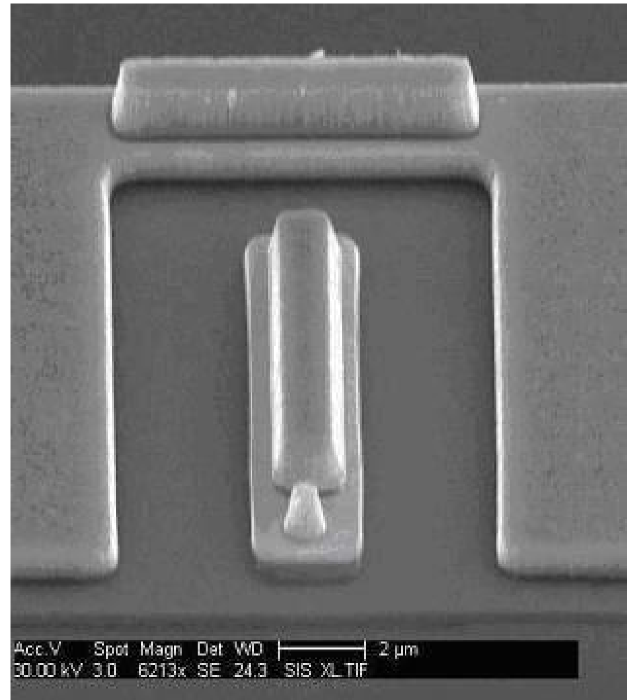
InP process, like other compound semiconductors, requires metal deposition and lift-off. Performing our AZ-5214E Image reversal photoresist standard lithography process on pieces requires special considerations. We decided to keep the photoresist on the carrier wafer to protect the delicate alignment marks during evaporation. To do that, we choose to expose only the mounted piece with patterns leaving the carrier wafer unexposed. After the reversal bake, we perform the flood exposure in the mask aligner. Normally this exposure causes the removal of this photoresist from the carrier wafer. We created a black film shield with a designated opening for the mounted piece that covers the carrier wafer only. This simple solution keeps the photoresist protection on the carrier wafer. Similar protection is given during evaporation. This time we use Gel-Pak® film that has designated opening for the piece only. Keeping the piece in the same location and size allows multi use of these Gel-Pak® films.

For positive photoresist, no special treatment is necessary.

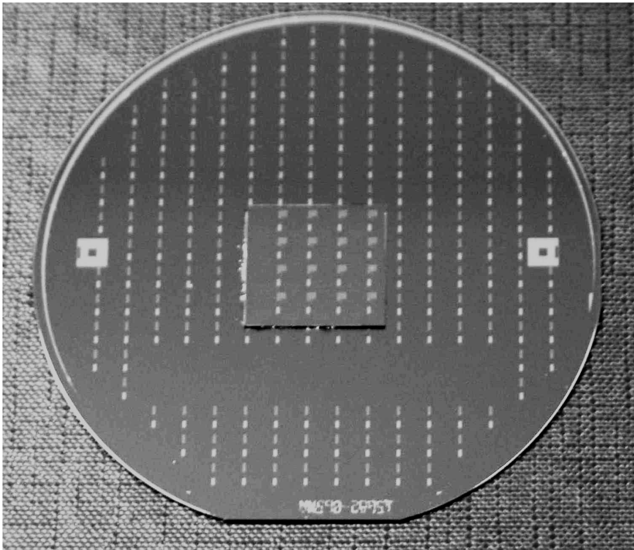
In all other processes the InP-mounted piece is treated as standard in-line wafer in standard FAB tools.

## CONCLUSIONS

We have achieved a way to perform a stepper based integrated process on InP pieces to create HBT (picture 1). This method allows us to perform preliminary R&D phase in a low-cost manner. This method can be modified to include other materials and technologies as well, extending the use of in-line FAB tools.




PICTURE 1. SEM image of HBT transistor manufactured on InP piece



PICTURE 2. InP piece after collector metal lift-off.


## ACKNOWLEDGEMENTS

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## ACRONYMS

R&D: Research and Development

CD: Critical Dimensions

DOF: Depth of Focus

HBT: Heterojunction Bipolar Transistor