Study of Thermal Coupling Effect in GaAs Heterojunction Bipolar Transistors by Using Simple Current Mirror Circuit

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Abstract

A simple method for determining the mutual thermal coupling resistance between adjacent heterojunction bipolar transistors (HBTs) in a GaAs integrated circuit (IC) is presented. It utilizes a simple current mirror (CM) configuration as a test vehicle to evaluate the electro-thermal interaction between two HBTs by comparing measured IV curves of the current mirror with circuit simulations that include the thermal coupling. By changing the distance between the two HBTs, the spatial dependence of the thermal coupling resistance is also determined. Comparing the measured data to theoretical calculations demonstrates that the interconnecting gold metal layers play an important role in thermal coupling.

INTRODUCTION

GaAs HBTs are key technology drivers in power amplifiers (PA), used in wireless communications. However, due to high power operation, small die size, and relatively low thermal conductivity substrates, electro-thermal issues are an important aspect of circuit and device design in this technology. Self-heating and device thermal resistance of HBTs are important considerations in the design of GaAs ICs and have been widely studied [1-3]. The thermal coupling (thermal effect to an adjacent device) is another important aspect [4], and a few studies have been published that consider both GaAs and metal layer effects [5, 6]. The thermal coupling is a phenomenon in which the temperature of a device is changed by power dissipation of neighboring devices. This temperature rise alters the bias point of the device and, consequently, changes its electrical performance. This electro-thermal coupling complicates the simulation and design of many GaAs circuits. Similar to a device thermal resistance R_{th}, which is used to quantify self-heating, the mutual thermal coupling resistance R_{th_21} is used to quantify the static mutual thermal coupling between devices, and it is defined as the ratio of temperature change in device ***(e.g. the reference transistor)*** to the power consumed by a neighboring device ***(e.g. source transistor)***. To provide good circuit and device design guidance for the thermal coupling related issues, a systematic way of characterizing this effect in an IC environment is needed. In this paper, a simple method, for measuring thermal coupling by monitoring the change in collector current using simple current mirror (CM) circuits, is presented. Because of passive nature of GaAs substrate R_{th_21} and R_{th_12} are equal, and we only use R_{th_21} to represent the mutual thermal coupling resistance in this paper. In addition, current mirror circuits are widely used in PA on-chip bias circuit designs, the understanding gained from this study of thermal coupling behavior directly benefits commercial HBT PA design.

DEVICE DESCRIPTION AND TEST RESULTS

The simplest current mirror circuit consists of two HBT devices with their base terminals connected together, to a reference terminal, and their emitters are connected on chip through a wide interconnect gold layer and grounded (see Fig. 1). The on-chip connection between two HBT emitter terminals will eliminate contact resistance difference due to probe contact at wafer level testing. The collector of one of the HBTs (the reference device) is also connected to the reference terminal. The collector of the other HBT (the source device) is connected to a voltage source, V_c, and I_c is the collector current of this source device. One source measurement unit (SMU) is connected to the reference terminal and the current, I_{ref}, is swept.

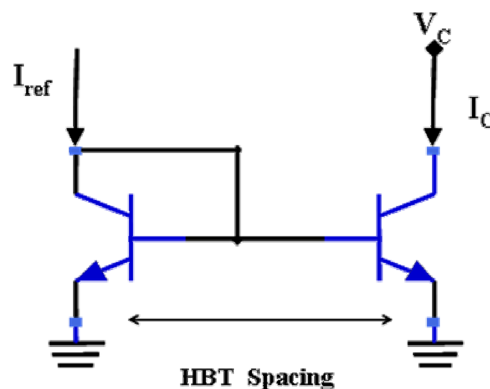

Figure 1. A simple current mirror circuit made of HBTs. Different spacings between HBT in current mirror circuit result in different degrees of thermal coupling.

At low current and low V_c voltage level, HBT power consumption induced temperature difference is minimum and can be neglected. The collector current, I_c, of the source device tracks the reference current, I_{ref}, linearly for a given V_c voltage. The ratio of the currents in the source and reference transistors can be calculated by Eq. (1) [7],

$$\frac{I_c}{I_{ref}} = \frac{A_{source}}{A_{ref}} \cdot \left[\frac{1}{1+\frac{1}{\beta_F}\left[1+\frac{A_{source}}{A_{ref}}\right]} \right] \cdot \left[\frac{1+V_{CE}/V_A}{1+V_{BE}/V_A} \right] \quad \text{Eq. (1)}$$

where I_c is source HBT collector current, I_{ref} is current through the reference terminal; A_{source} and A_{ref} are areas of the source and reference HBTs. β_F and V_A represent HBT current gain and early voltage; V_{CE} and V_{BE} represent the collector emitter junction voltage of the source and reference HBTs. Since the absolute values of HBT early voltage and current gain are very large (in the order of 100), the current ratio in Eq. (1) can be simplified to HBTs' area ratio. However, as the reference current, I_{ref}, or the collector voltage, V_c, increases further, the power dissipation, and consequently the device temperature, in the source device, increases significantly. Thermal effects become important and the collector current, I_c, of the source device no longer tracks I_{ref} linearly. In these cases, Eq. (1) becomes invalid and circuit simulation becomes necessary to predict circuit behaviors.

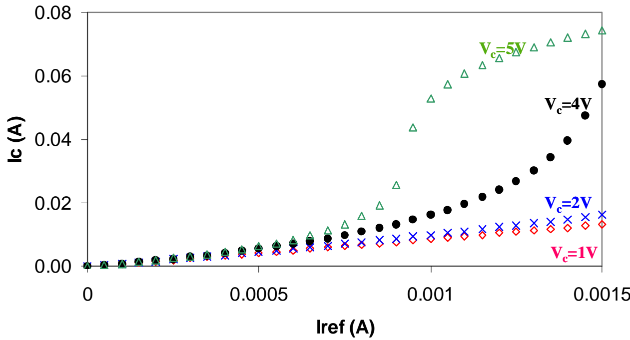

Figure 2. Measured collector current I_c vs reference current I_{ref} of a HBT current mirror circuit. The emitter areas of reference HBT and source HBT are 12um^2 and 120um^2, respectively. The spacing between them is 50 µm. Only I_c at V_c=1V, 2V, 4V and 5V were plotted.

In circuit simulation, both self-heating and thermal coupling have to be included in order to accurately simulate the dependence of the collector current of the source device on both V_c and I_{ref}. Taking advantage of the fact that HBT thermal resistance and capacitance (R_{th} & C_{th}) are properly included in most current compact models, the thermal coupling resistance can be well determined by adding a thermal coupling network, including the thermal coupling resistance, in the simulation.

In this work two sets of HBT current mirror (CM) circuits were studied. One set of circuits, q12/q120 CM, consists of HBTs with emitter areas of 12 µm^2 and 120 µm^2 for the reference and source devices, respectively. Spacings of 26 µm, 50 µm, 90 µm and 162 µm were used. The second set of circuits, q60/q120 CM, used HBTs with emitter areas of 60 µm^2 and 120 µm^2, for the reference and source devices, respectively. This set of circuits consists of 31 µm, 60 µm, 100 µm and 150 µm spacings. The testing was performed at room temperature on wafers with a thickness of 100 µm. An HP4142B Modular DC Source / Monitor was used to conduct the tests. The collector V_c voltage was stepped from 1V to 5V for the q12/q120 CM and to 4V for the q60/q120 CM in 0.5V increments for each I_{ref} sweep. I_{ref} was swept from 0 mA to 2 mA for the q12/q120 CM circuits and from 0 mA to 30 mA for q60/q120 CM circuits. Fig. 2 shows an example of the measured I-V curves for q12/q120 with 50 µm spacing. The observed features are typical of the studied CM circuits. At low I_c and V_c range, such as V_c less than 2V and I_{ref} less than 0.5mA, I_c increases linearly with I_{ref}. Above such range nonlinear features appear in the curves. At a fixed large V_c voltage, different spacings between HBT in CM circuit result in different degrees of thermal coupling. It is reflected in I_c current nonlinearity in CM circuit. Fig. 3 shows a set of I_c current at V_c=4V in q12/q120 CM having HBT separated by 26µm, 50µm, 90µm, and 162µm separately. It shows I_c current variation for different HBT separations. I_c currents from the same set of q12/q120 CM at V_c =1V were plotted in the same figure for comparison. Such a spatial dependence of nonlinear feature provides us opportunity to deduce the spatial dependence of thermal coupling resistance R_{th_21} through comparison between measurement data and circuit simulation results.

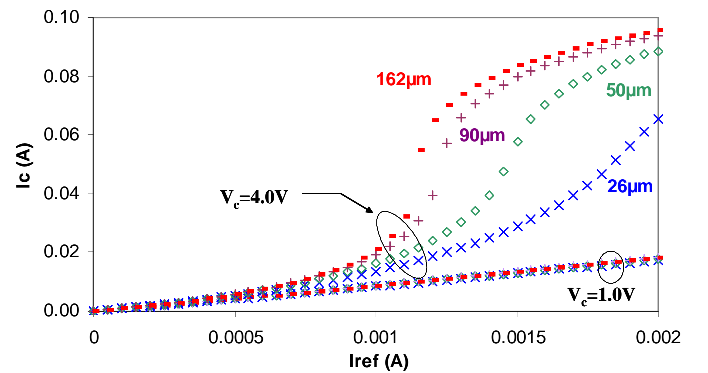

Figure 3. Measured collector current I_c vs reference current I_{ref} of q12/q120 CM circuits having HBT spacing 26µm, 50µm, 90µm, and 162µm separately. Only I_c curves at V_c=1V and V_c=4V are plotted.

To simulate the measurement results, we used Agilent Advanced Design System (ADS) in the circuit simulation. During the simulation the power consumption of each HBT at each biasing point was calculated. The powers were converted into the junction temperature rise for each device

using the thermal resistance and the thermal coupling resistance. The temperature dependence of a HBTs' base-emitter turn-on voltage is well known (about -1.3mV/°C) [8], so the temperature rise at a particular HBT bias point can be calculated. The thermal coupling resistance is determined by iterating the value of thermal coupling resistance (in simulation) to obtain the best fit between the simulated and measured I-V curves. Figure 4 displays the measured and simulated results of q12/q120 CM with 26µm separation between HBTs.

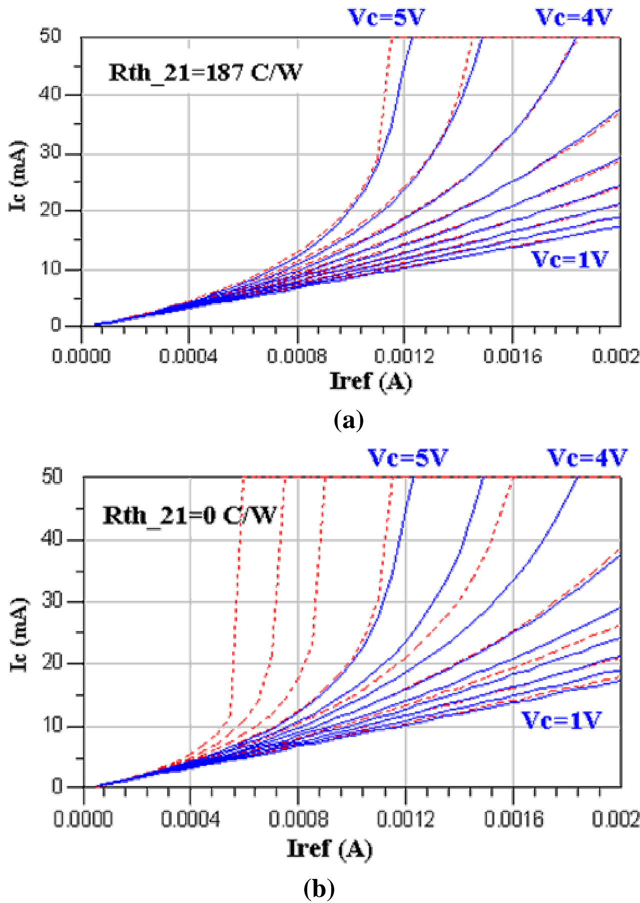

Figure 4. Measured (—) vs simulated (---) I_c currents (a) with and (b) without including thermal coupling resistance for q12/q120 CM circuit in ADS simulation. The HBTs separation is 26µm.

These simulations show a significant difference between properly including R_{th_21} and simply neglecting R_{th_21}. Applying this procedure to all of the current mirrors, with devices at varying distances, the spatial dependence of the thermal coupling resistance was determined. Fig. 5 shows experimentally deduced thermal coupling resistance of two sets of CM circuit (bold dot symbols for q12/q120 CM and solid diamond symbols for q60/q120 CM). A general trend of decreasing thermal coupling resistance with increasing distance between HBTs is observed. In other words, the thermal interaction of two HBTs becomes weaker as the spacing between them gets larger.

The theoretical calculation of thermal coupling resistance was performed using an in-house thermal analysis program based on an analytical solution to the heat equation. The in-house program was validated by a commercial 3D thermal simulation CAD tool. However the program does not include the effect of interconnecting metal layers. The calculated results are displayed in Fig. 5 also as a thick solid line in the bottom. Compared to the experimental thermal coupling resistance, the theoretically calculated values are very small.

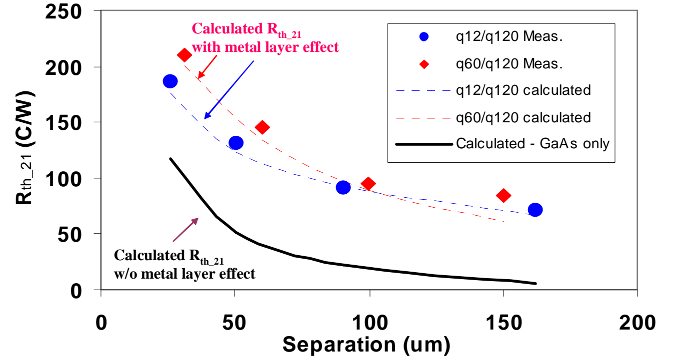

Figure 5. Measured thermal coupling resistances of q12/q120 CM (●)and q60/q120 CM (◆), calculated thermal coupling resistance (—) without including gold metal layer effect, and calculated ones including gold metal layer effect (---, ---).

The cause of this discrepancy is due to neglecting the gold interconnect metal layer between two HBTs. Using published values for the thermal conductivity with the dimensions of the gold metal interconnect in CM circuit layout, the gold interconnect layer's contribution to the thermal resistance between the two HBTs can be calculated. The gold layer thermal resistance and GaAs substrate related thermal resistance between two HBT are in parallel connection. The final thermal network can be simplified as a pi-network showed in Fig. 6. In the figure R_A and R_C represent effective lumped thermal resistance associated with source and reference HBTs respectively. Their values can be approximated to the measured self-heating thermal resistance of source and reference HBTs in our cases. R_B represents the combined thermal resistance of gold metal layer and GaAs substrate (R_B is not R_{th_21}). The final thermal coupling resistance can be expressed as Eq. (2) by applying R_{th_21} definition into the pi-network in Fig. 6 [8, 9].

$$R_{th_21} = \frac{R_A \bullet R_C}{R_A + R_B + R_C} \qquad \text{Eq. (2)}$$

where R_A, R_C represent two thermal resistance in the network, and R_B represents the combined thermal resistance of gold metal layer and GaAs substrate between HBTs. The calculated thermal coupling resistances R_{th_21} are re-plotted in fine dash lines in Fig. 5 for two sets of circuits. The calculation including the effect of metallization shows

very good agreement with the experimental data. This result indicates that standard gold metal interconnect plays a significant role in the thermal coupling in GaAs ICs. This work demonstrates the feasibility of using the gold interconnect metal to enhance the thermal coupling between devices. It also shows that interconnect metal related thermal coupling effect cannot be simply ignored in simulation of GaAs circuits.

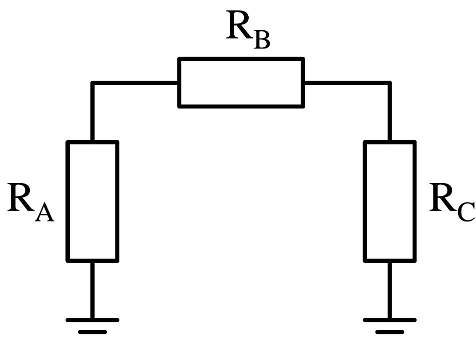

Figure 6. A simplified thermal network of current mirror circuit for the calculation of final thermal coupling resistance, R_{th_21}. R_B represents combined thermal resistance of gold metal layer and GaAs substrate between two HBTs.

CONCLUSIONS

In conclusion, a simple method to deduce thermal coupling resistance between HBTs in GaAs IC's was presented. The setup is very simple and only requires DC Source / Monitor units. A drawback of this method is that it only provides the real part of the thermal coupling, which is still important for DC operation (bias point determination). The work demonstrates the importance of the gold metal layer in thermal coupling determination, and it highlights the feasibility of using gold interconnects to enhance the thermal coupling between devices.

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