

# Production Ready Ultra High Breakdown 6" pHEMT Technology

Cheng-Guan Yuan, Y. Y. Hsieh, T. J. Yeh, Chung-Hsu Chen, D. W. Tu, Yu-Chi Wang, Joe Liu  
Saad Murad<sup>#</sup>, Ramon Schook<sup>#</sup>, Frans Bontekoe<sup>#</sup>, and Mark Tomesen<sup>#</sup>

Win Semiconductors Corp. N 69 Technology 7<sup>th</sup> Rd, Hwaya Technology Park, Kuei Shan Hsiang,  
Tao Yuan Shien, Taiwan (333)

<sup>#</sup>Philips Semiconductors B.V. Gerstweg 2, 6534 AE, Nijmegen, The Netherlands

## Abstract

**A production ready pseudomorphic high electron mobility transistor (pHEMT) with high breakdown voltage, improved 1/f noise, and linearity has been developed. This technology shows better than 35V breakdown voltage uniformly across 6-inch wafers. The high performance circuits are demonstrated with 0.5 μm pHEMT process. This PHEMT technology is ready for high volume production with low cost.**

## I. Introduction

Cable TV power amplifiers require high linearity devices that can minimize intermodulation distortion products, at the same time, need high breakdown voltage of more than 24V. To date, gallium arsenide-based pHEMTs have demonstrated better gain with low distortion and low noise. Therefore, the use of GaAs pHEMTs is desirable for applications that require high linearity and low noise simultaneously.

The major parameters in CATV specification to determine a pass/fail are the linearity characteristics in terms of CTB (Composite Triple Beat) and CSO (Composite Second Order). The specification demands not only good linearity but also high stability of this linearity.

In this paper, we report the development of a high breakdown GaAs/AlGaAs/InGaAs pHEMT for the monolithic cable TV power amplifier IC. Cost-effective foundry process has been designed for reduced processing step, and at the same time achieving high performance.

## II. Device and Process

The pHEMT devices utilize molecular beam epitaxy (MBE) grown material on 6-inch GaAs substrate. InGaAs channel, and two etch stop layers for selective etching of wide recess and gate recess.

The structure of the epitaxy consists of a thin, undoped InGaAs channel layer, with high Indium concentration (15%). Double delta-doped layers

provide carriers to the channel. The front to back pulse dope ratio is 2.5. AlGaAs spacer layers are grown between the channel layer and the Si pulse-doped layers. An AlGaAs Schottky layer is placed on top of the upper spacer layer.

The cross section of a 0.5 μm gate-width device is sketched in Figure 1. The field plate extends from gate to drain. In this field-plate device, the electric field originating from the extension portion of the gate contributes to the formation of the depletion region in the passivation and conducting channel layers between the gate and drain. This is equivalent to providing additional depletion area at channel, resulting in a low electric field peak at the drain-side edge of the gate.<sup>1</sup>

For device processing, ohmic patterns were defined by stepper lithography and Au/Ge/Ni/Au metals were evaporated in the contact regions in order to have good ohmic contact, and sintering was performed using rapid thermal annealing with optimized conditions. Low contact resistance ( $R_c$ ) of 0.18 Ω-mm is achieved. After wide recess step, the 0.5μm gate was defined by optical lithography. The gate level was completed by Ti/Pt/Au evaporation. The gate recess profile was controlled by wet-etch process. After the gate definition, the device was fully passivated by SiN of 1100Å thick. For passive components, the TaN resistor with sheet resistance 50±1Ω/sqr was fabricated. The MIM capacitor has a capacitance of 500±50 pF/mm<sup>2</sup>.

## III. Device Performances and Characteristics

### ● Highly Uniform Production Wafers

The typical  $I_{ds}$ - $V_{ds}$  relationship is presented in Figure 2. The  $V_{gs}$  is biased from -1.3V to -0.2V with 0.1V as a step; and the  $V_{ds}$  varies from 0V and 20V. The MIM capacitor has a capacitance of 500 pF/mm<sup>2</sup>, and the on-state resistance,  $R_{on}$ , is 2.9Ω-mm, which is defined at  $V_{gs}=0.5V$ . The typical transfer curve is shown in Figure 3. The drain-to-source voltage is 3V,

and the  $V_{gs}$  steps from -1.5V to 0.5V. As shown in Figure 4, the pinch-off voltage is typically -1.1V across a wafer, defined at drain current of 0.1mA/mm, with a standard deviation of 0.02V. As demonstrated in Figure 5, the drain current density at  $V_{gs}=0V$  is 260mA/mm, and the saturation drain current density at  $V_{gs}=0.5V$  and  $V_{ds}=3V$  is 330mA/mm. Typical DC and RF parameters for our devices are given in Table 1.

The minimum drain-to-gate breakdown voltage BVDGO is higher than 35V. This is defined at  $I_g=0.1mA/mm$ . As shown in Figure 6, wafers with highly uniform across-wafer gate-drain breakdown voltage have been manufactured. The standard deviation of 1.6V across a 6-inch wafer is considered to be excellent for the targeted application.

Furthermore, as shown in Figure 7, very dense SiN, with breakdown higher than 100V, is used for MIM capacitors. Therefore, leakage current is greatly reduced.

#### ● **1/f Noise Performance**

The concentration of defect centers, known as DX centers, in the AlGaAs Schottky layer of a pHEMT epitaxial layer structure could play an important role in the 1/f noise level. By improving the epitaxial material quality with reduced defect centers, the 1/f noise should be reduced. Minimizing the effect from surface trapped charge is another well-known solution to improve the 1/f noise. This can be achieved by optimizing process, and reducing the surface state charge between the silicon nitride and semiconductor interface. For  $50\mu m \times 4$ -finger transistors biased at  $I_{ds}=100mA/mm$ , the noise figure is around 4.3dB at 50MHz, as shown in Figure 8.

#### ● **Bare-Die HAST Stability Test**

The final protect nitride has been proven to be reliable under HAST condition of 132°C, 96hr and 85% humidity.

#### ● **Bell Shape Gate Current**

The bell-shape gate current is believed to come from the impact ionization.<sup>2,3</sup> To prevent it from device characteristics, either the carrier density should be minimized or the longitudinal electric field from drain to source should be lowered by the critical impact ionization field. As shown in Figure 9, field plate is found to be an effective way to suppress the gate leakage at high drain voltage and drain current.

The devices with field plate show smaller bell shape gate leakage than those without field plate.

### **III. Product Applications**

#### ● **Operation Stability Test (OST)**

The degradation of electrical characteristics, such as breakdown voltage, surface leakage, pinch-off voltage, or Schottky barrier height, might be related to stress of passivation.

The linearity degradation under OST condition is due to the change of both passivation and gate recess region on the drain side. The approaches for OST stability improvement basically are two folds. Firstly, it is essential to utilize stable passivation. Secondly, it is always preferred to optimize process sequence to prevent high-stress and high temperature induced reaction at GaAs-SiN interface, especially in the recess region.

#### ● **CATV Power Amplifier applications**

Good linearity at high output power, low noise and high device reliability are design-challenging for infrastructure Cable TV power amplifiers. Enabling technology is critical to cover for the variety of CATV amplifier types in the network, from trunks, to high power bridger amplifiers to line extenders feeding the home connections. In Figure 10 and Figure 11, results are shown of measured CTB and CSO values of bridger amplifiers. A performance comparison is made on devices, designed in WIN/pHEMT versus three state-of-the art products available on the market today [Comp#1,2,3]. The graphs show that improved linearity, uniformly over the frequency band, is obtained for devices using this new pHEMT technology [Type UGD10420].

### **IV. Summary and Conclusions**

In conclusion, a cost-effective and excellent uniformity 35V pHEMT MMIC process is presented in this paper.

Various nitrides to achieve stable passivation, high breakdown MIMCAP, and HAST resistant protection have been developed. The optimization study has met both HAST and OST requirements. A high breakdown 6" pHEMT process technology is ready for production.

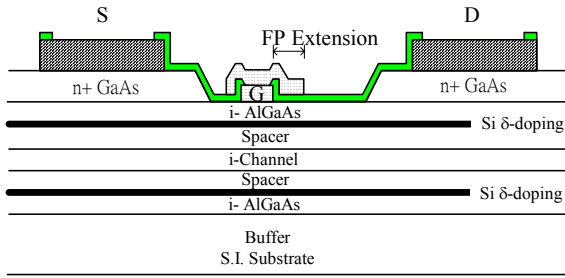


Figure 1. Cross section of 0.5 μm pHEMT device.

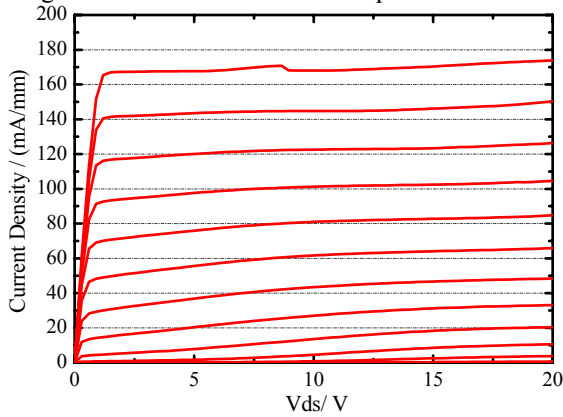


Figure 2. Typical I-V characteristics of WIN 0.5 μm high breakdown power pHEMT technology.

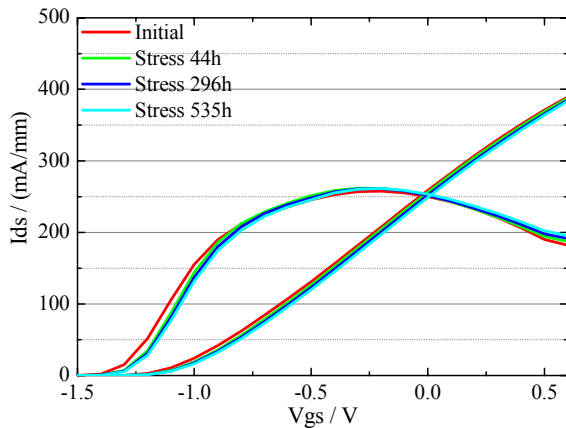


Figure 3. Typical  $G_m$  &  $I_{ds}$  curves of WIN 0.5 μm high breakdown power pHEMT technology.

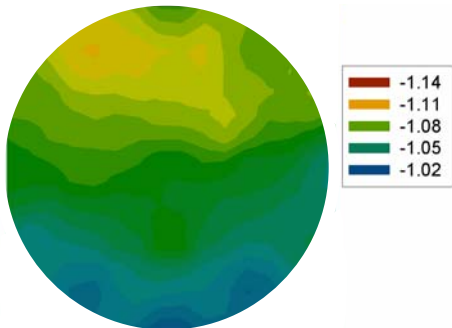


Figure 4. Wafer map of 6-in wafer. The pinch-off voltage is -1.1V with a standard deviation of 0.02V across wafer.

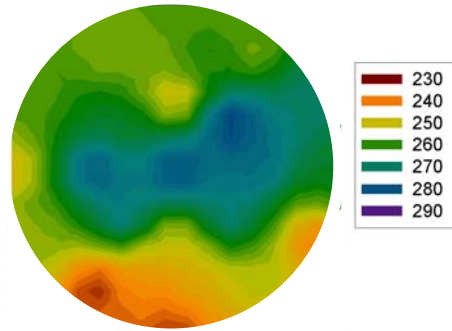


Figure 5. Wafer map of 6-in wafer. The drain current density at  $V_{gs}=0V$  is 260mA/mm with a standard deviation of 14mA/mm across wafer

Table 1. Typical values of DC device parameters measured on a single finger 150μm wide FET.

Parameter	Symbol	Value	Unit
Breakdown voltage between Gate-Drain	BVDGO	> 35	V
MIM Capacitance	CP OO YM	500	pF/mm <sup>2</sup>
Cut-off frequency @ $V_{ds}=1.5$ volt	ft	21	GHz
$I_{ds}@V_{gs}=0.5$ volt, $V_{ds}=1.5V$	$I_{dmax}$	420	mA/mm
$I_{ds}@V_{gs}=0$ volt, $V_{ds}=1.5V$	$I_{DSS}$	315	mA/mm
TLM epi sheet resistance	RS TL EP	170	ohm/sq
TLM TFR sheet resistance	RS TL TR	50	ohm/sq
Pinch-off voltage	VPO	-1.1	V

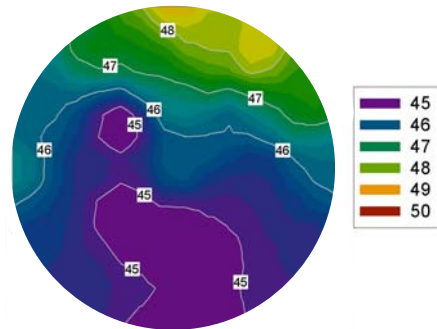


Figure 6. Wafer map of 6-in wafer. Highly uniform gate-drain breakdown voltage. (Avg.: 46V, StDev: 1.6V)

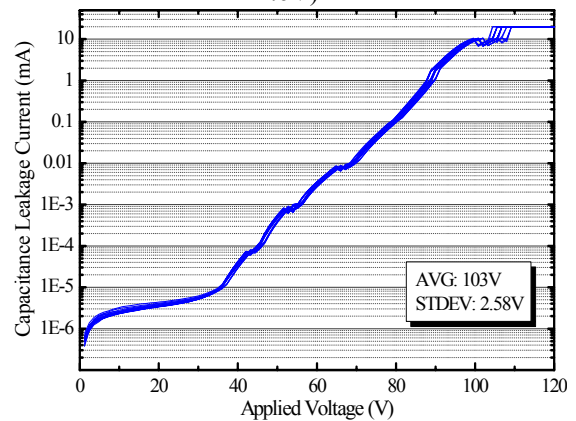


Figure 7. Capacitor breakdown (average >100V, standard deviation <2.5V).

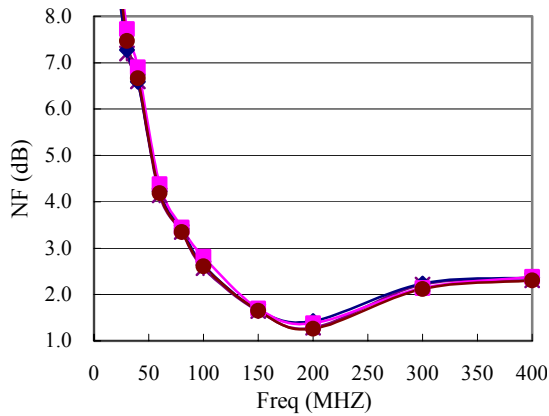


Figure 8. 1/f Noise performance of WIN 0.5  $\mu\text{m}$  high breakdown pHEMT technology.

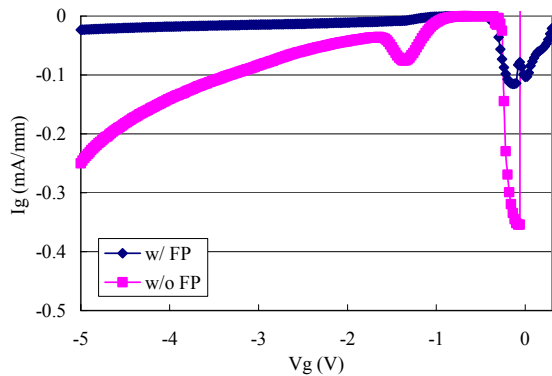


Figure 9. Field plate is found to be an effective way to suppress the gate leakage. The devices w/ field plate show smaller bell shape than those w/o field plate.  $V_d=12\text{V}$

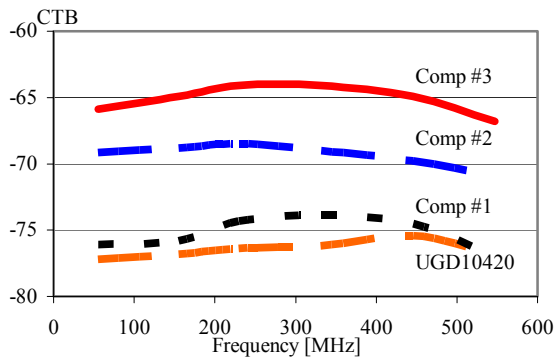


Figure 10. CTB values of bridger amplifiers.

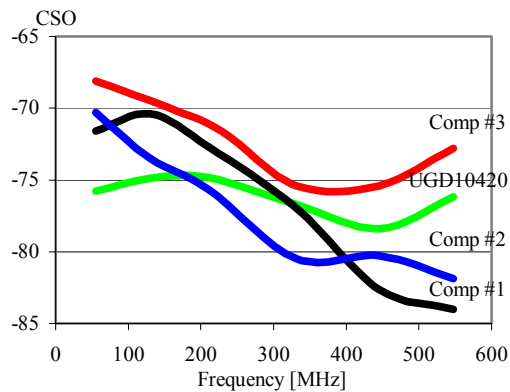


Figure 11. CSO values of bridger amplifiers.

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## References

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