From Epitaxy to Backside Process: Reproducible AlGaN/GaN HEMT Technology for Reliable and Rugged Power Devices

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Abstract

We report on a reproducible 3″ GaN HEMT technology showing good device performance and reliability. AlGaN/GaN HEMT structures are grown on semi-insulating SiC substrates by MOCVD with sheet resistance uniformities better than 3%. Device fabrication is performed using standard processing techniques involving both e-beam and stepper lithography. The process technology exhibits an excellent uniformity across a single wafer and a high reproducibility between individual wafers of the same or a different batch. Good performance is shown at different examples, such as large power bars for 2 GHz frequency as well as MMICs running at 18 GHz. Reliability tests are performed at both radio frequency (RF) and direct current (DC) stress conditions and indicate promising device stability.

INTRODUCTION

Group III nitrides have found to be well suited for high temperature and high power applications, due to their wide band gap, high breakdown field, current density and saturation velocity. We report on a powerful technology well-matched to the requirements of a large variety of applications ranking from RF to millimeter wave frequencies for both large power bar high electron mobility transistors (HEMTs) as well as monolithic microwave integrated circuits (MMICs).

TECHNOLOGY

AlGaN/GaN heterostructures are grown on semi-insulating SiC substrates by metal organic chemical vapor deposition. Incoming substrate wafers are classified using polarized light imaging in order to examine their defect distribution. Epitaxial growth starts with an AlN nucleation layer followed by a thick GaN buffer layer and the AlGaN/GaN barrier. The growth procedure is optimized for a highly insulating buffer as well as low trap densities. E.g. for a 22 nm $Al_{0.22}Ga_{0.78}N$ barrier and a 3 nm thin GaN cap typical sheet carrier concentration and mobility are 8×10^{12} cm^{-2} and 1500 cm^2/Vs yielding sheet resistances around 500 Ω/sq that are reproducibly obtained with a uniformity better than 3% across the entire wafer. Up to twelve 3-inch SiC wafers can be loaded into one epitaxy batch. The threading dislocation density is in the low 10^8 cm^{-2} range as determined by plane view transmission electron microscopy. The buffer isolation resistance at 60 V is well above 10^{12} Ω/sq for a 4 µm gap test structure.

Processing is performed in microstrip line technology consisting of frontside processing, substrate thinning down to 100 µm, and backside processing including front-to-back substrate via holes. Standard gate lengths of our HEMTs are 0.25 µm and 0.50 µm, depending on the specific application, in combination with thin film resistors, high-voltage capacitors and inductors for impedance matching to a 50 Ω environment. Standard processing techniques are used involving electron-beam and optical lithography: Stepper alignment for frontside and contact mask alignment for backside device definition. The whole technology sequence is subject of a continuous improvement process with the main focus on reduction of leakage currents and low frequency dispersion, increase of breakdown voltages and simultaneously improving the overall RF performance and reliability. This is mainly achieved by a combination of epitaxial growth optimization as well as modifications in the passivation nitride and the gate module. Every process module in the technology sequence has been optimized to insure its reproducibility and is subject of a permanent monitoring procedure. For the backside process, the thermal management has been a subject of development to avoid a performance degradation of the devices. By introducing these measures, the process technology presented here leads to a

good uniformity across a single wafer as well as to a high reproducibility from wafer to wafer.

RESULTS

Power HEMTs have both high PAE (power added efficiency) and low leakage currents, thus demonstrating that we have successfully achieved high isolation and low trap densities. Continuous wave loadpull power sweep wafer mapping of a 0.8 mm gate width structure without intentional harmonic matching across all 21 cells on an entire 3-inch wafer (Figure 1) yields a PAE of (68±2)% per single wafer measured at 50 V. The high level of reproducibility is demonstrated in a comparison of these values on a total of 21 engineering batches, where more than 100 wafers are involved (Figure 2).

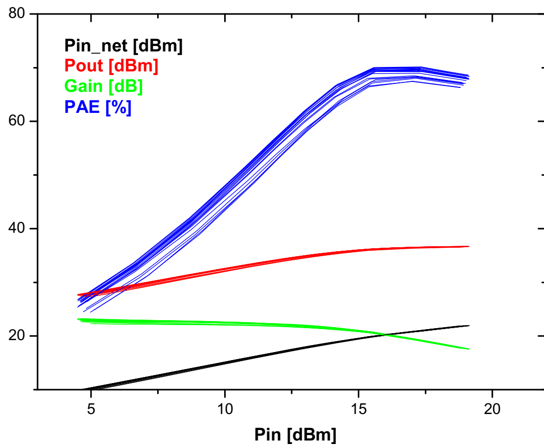

Figure 1: Example of a 2 GHz load pull power sweep wafer mapping overlay at 50 V of 0.5 µm gate length HEMTs with 0.8 mm gate width across all 21 cells of an entire 3 inch wafer.

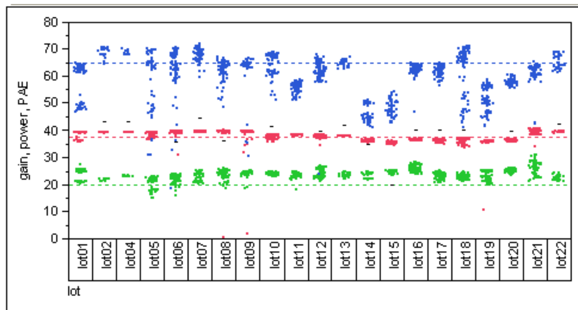

Figure 2: Gain (green, bottom) [dB], output power (red, middle) [dBm] and PAE (blue, top) [%] of a total of 21 engineering lots (> 100 wafers) as determined from 2 GHz load pull mapping. Variations in PAE data refer to different epitaxial structures.

Dynamic evaluation circuits (DECs) are used to monitor the high frequency parameters of our HEMTs. As an example, a photo of such a monitor is presented in figure 3, which has been processed with microstrip lines and back side vias.

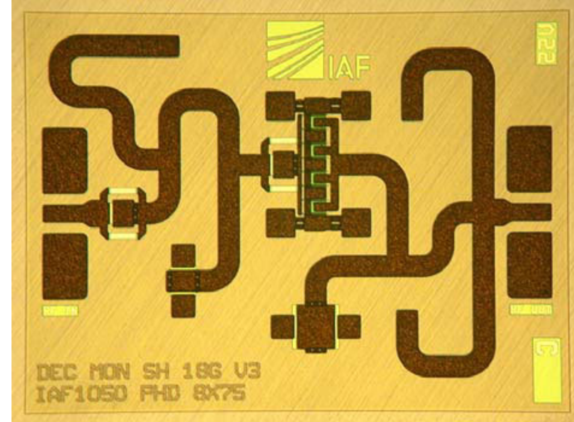

Figure 3: Photo of a 18 GHz DEC monitor with 0.25 µm gate technology. Chip size is 2 x 1.5 mm^2

Figure 4 shows the frequency dependent small signal properties of a DEC operating at 28 V, which has been fabricated in 0.25 µm gate length technology with a total gate width of 600 µm (8 x 75 µm). The measurement shows a good performance over the bandwidth from 16 GHz to 20 GHz and indicates an excellent homogeneity of the active device as well as of the passive matching network across a complete 3-inch wafer.

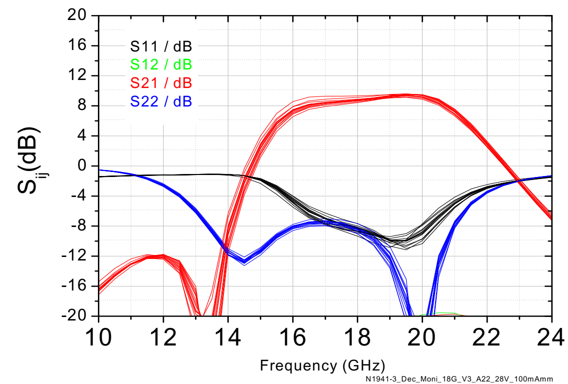

Figure 4: Small signal mapping overlay across a 3 inch wafer of a 18 GHz DEC monitor with 0.25 µm gate technology measured at 28 V drain bias (red, top: S_{21}, blue: S_{22}, black: S_{11}) , demonstrating the excellent process homogeneity.

Reliability

Reliability tests are performed first on wafer as short screening tests, such as HTRB or Idq stress, and also on packaged devices with various gate peripheries. Both DC and RF tests are carried out. As an example shown here the reliability of our MMIC technology has been investigated using single stage amplifiers with a gate length of 0.25 µm and a total gate width of 1 mm (8 x 125 µm) which have been mounted in a RF package and stressed at a frequency of 10 GHz. The reliability is very promising. The amplifiers have been measured at 42 V in 2 dB compression. They work stable for more than 3000 h at a channel temperature of 236°C, which has been calibrated by the Raman method. Further increase of the device temperature to more than 250°C leads to degradation in gain. The average lifetime at working conditions was calculated based on a failure criterion of -1dB loss in gain. Based on eight devices and 18,000 h of cumulative stress time an activation energy of

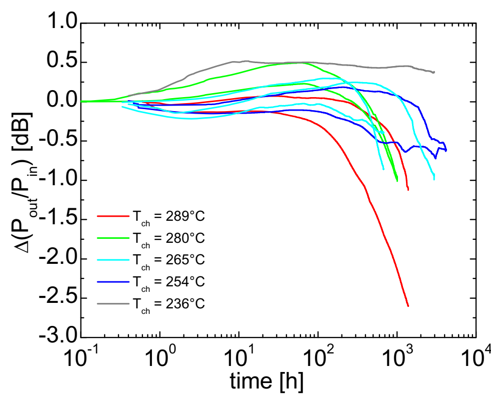

Figure 5: Gain degradation during 10 GHz stress test of single stage amplifiers at different channel temperatures at a drain voltage of 42 V. [T= 236°C upper curve, T= 289°C lowest curve]

1.7 eV and a median lifetime of 5×10^5 h at a channel temperature of 200°C has been estimated from the Arrhenius Plot shown in Figure 6. Future work will include the physical investigation of the degradation mechanism and the study of the reproducibility of this very encouraging result for wafers from different lots.

Conclusion

We have developed a powerful and reproducible microstrip line technology for AlGaN/ GaN HEMT devices and circuits for a large variety of applications. The overall performance of the devices exhibits excellent homogeneity and reproducibility. Reliability test under both DC and RF conditions reveal a promising long term stability of the devices.

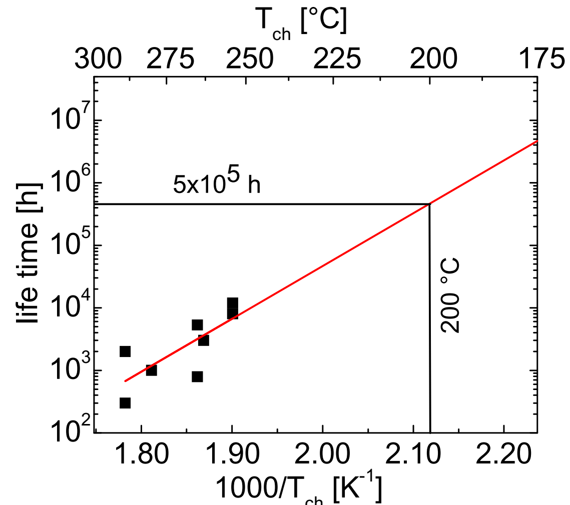

Figure 6: Arrhenius plot of single stage amplifiers at stress condition 10 GHz, 42 V and 2 dB compression. The failure criterion has been -1 dB degradation of gain, leading to an activation energy of Ea = 1.7 eV. The extrapolated life time can be calculated as 5×10^5 h at $T_{channel}$ = 200°C. The channel temperature has been measured by Raman method.

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Acronyms

HEMT: High electron mobility transistor
GaN: Gallium nitride
AlGaN: Aluminium gallium nitride
MOCVD: Metal-organic chemical vapor deposition
PAE: Power added efficiency
HTRB: High temperature reverse bias
MMIC: Monolithic microwave integrated circuit
DEC: Dynamic evaluation circuit